CLAIMS

What is claimed is:

1. A method for supporting digital signal processing (DSP) of a plurality of data types, the method comprising the steps of:

continuously broadcasting a plurality of firmware algorithms to a plurality of DSP engines over a channelized serial bus; and

selectively monitoring for and receiving at least one firmware algorithm of the plurality of firmware algorithms by at least one of the plurality of DSP engines, wherein the at least one firmware algorithm is used to process data of at least one corresponding data type received by the at least one of the plurality of DSP engines over at least one data line.

2. The method of claim 1, further comprising the steps of:

receiving at least one pulse coded modulation (PCM) data stream from a public switched telephone network (PSTN);

generating at least one packet of data from the PCM data stream using the received at least one firmware algorithm; and

transmitting the at least one packet of data over an Internet Protocol (IP) network.

3. The method of claim 1, further comprising the steps of:

receiving at least one packet of data from an IP network;

generating at least one PCM data stream from the at least one packet of data using the at least one firmware algorithm; and

transmitting the at least one PCM data stream over a PSTN.

4. The method of claim 1, wherein the at least one data line comprises at least one bidirectional PCM data stream.

5. The method of claim 1, wherein the at least one data line comprises at least one bidirectional host bus.

6. The method of claim 1, wherein the plurality of firmware algorithms are continuously broadcasted to a plurality of service DSP engines by a master DSP engine resident in a processor.

7. The method of claim 6, wherein the channelized serial bus comprises eight channels.

8. The method of claim 7, wherein the step of selectively monitoring for and receiving at least one firmware algorithm comprises the steps of:

determining a data type of the data received into at least one of the plurality of service DSP engines;

determining at least one firmware algorithm required to process the received data;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available.

9. The method of claim 8, wherein the step of selectively monitoring for and receiving at least one firmware algorithm further comprises the step of unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least

one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

10. The method of claim 9, wherein the step of selectively monitoring for and receiving at least one firmware algorithm further comprises the steps of:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

11. The method of claim 8, wherein each service DSP memory comprises data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted.

12. The method of claim 8, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is downloaded to each service DSP engine from the processor.

13. The method of claim 8, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is hard-coded in each of the service DSP engines.

14. The method of claim 7, wherein each channel of the channelized serial bus transmits at least one firmware algorithm.

15. The method of claim 6, wherein the plurality of firmware algorithms are stored in a memory of the master DSP engine.

16. The method of claim 1, wherein the continuous broadcast is repetitive.

17. The method of claim 1, wherein the plurality of data types comprise modem data, voice data, audio data, video data, and facsimile data.

18. The method of claim 1, wherein each DSP engine comprises at least one channel.

19. The method of claim 7, wherein at least one algorithm is transmitted on a channel of the channelized serial bus.

20. The method of claim 7, wherein an algorithm is transmitted using at least one channel of the channelized serial bus.

21. The method of claim 1, wherein each of the plurality of DSP engines comprise a memory for storing the at least one firmware algorithm.

22. The method of claim 1, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms.

23. The method of claim 22, wherein the at least one serial block comprises 1024 information bits.

24. The method of claim 22, wherein the broadcast of each of the at least one serial blocks is preceded by a broadcast of an address signal, the address signal identifying the firmware algorithm of the broadcasted at least one serial block.

25. An apparatus for supporting digital signal processing (DSP) of a plurality of data types, the apparatus comprising:

a serial bus comprising at least one channel over which a plurality of firmware algorithms are broadcasted; and

a plurality of DSP engines coupled to the serial bus and to at least one data line, at least one of the plurality of DSP engines selectively monitoring for and receiving at least one firmware algorithm of the plurality of firmware algorithms broadcasted, wherein the at least one firmware algorithm is used to process data received by the at least one of the plurality of DSP engines over the at least one data line.

26. The apparatus of claim 25, further comprising a master DSP engine resident in a host processor, the master DSP engine coupled to the serial bus, wherein the master DSP engine continuously broadcasts the plurality of firmware algorithms to a plurality of service DSP engines.

27. The apparatus of claim 26, wherein:

at least one pulse coded modulation (PCM) data stream is received from a public switched telephone network (PSTN);

at least one packet of data is generated from the PCM data stream using the received at least one firmware algorithm; and

the at least one packet of data is transmitted over an Internet Protocol (IP) network.

28. The apparatus of claim 26, wherein:

at least one packet of data is received from an IP network;

at least one PCM data stream is generated from the at least one packet of data using the at least one firmware algorithm; and

the at least one PCM data stream is transmitted over a PSTN.

29. The apparatus of claim 25, wherein the at least one data line comprises at least one bidirectional PCM data stream.

30. The apparatus of claim 25, wherein the at least one data line comprises at least one bidirectional host bus.

31. The apparatus of claim 26, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

determining a data type of the data received into at least one of the plurality of service DSP engines;

determining at least one firmware algorithm required to process the received data;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available.

32. The apparatus of claim 31, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

33. The apparatus of claim 32, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

34. The apparatus of claim 31, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is downloaded to each service DSP engine from the host processor.

35. The apparatus of claim 25, wherein the data received by the at least one of the plurality of DSP engines comprises at least one channel of multiplexed data received over a public switched telephone network, the data having at least one of the plurality of data types.

36. The apparatus of claim 25, wherein the plurality of data types comprise modem data, voice data, audio data, and facsimile data.

37. The apparatus of claim 25, wherein each DSP engine comprises at least one channel.

38. The apparatus of claim 26, wherein at least one algorithm is transmitted on a channel of the channelized serial bus.

39. The apparatus of claim 26, wherein an algorithm is transmitted using at least one channel of the channelized serial bus.

40. The apparatus of claim 25, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms, wherein the portion of each of each of the plurality of firmware algorithms comprises 1024 information bits.

41. A multiservice digital signal processing (DSP) system comprising:

a processor coupled to at least one data line, the processor comprising a master DSP engine, wherein the at least one data line provides a plurality of data types;

a serial bus coupled to the master DSP engine, the serial bus comprising a plurality of channels over which a plurality of firmware algorithms are continuously broadcasted; and

a plurality of service DSP engines coupled to the at least one data line and the serial bus, at least one of the plurality of service DSP engines

selectively monitoring for and receiving at least one firmware algorithm over the serial bus, wherein the at least one firmware algorithm is used to process data of at least one corresponding data type received by the at least one of the plurality of service DSP engines over the at least one data line.

42. The system of claim 41, wherein:

at least one pulse coded modulation (PCM) data stream is received from a public switched telephone network (PSTN);

at least one packet of data is generated from the PCM data stream using the received at least one firmware algorithm; and

the at least one packet of data is transmitted over an Internet Protocol (IP) network.

43. The system of claim 41, wherein:

at least one packet of data is received from an IP network;

at least one PCM data stream is generated from the at least one packet of data using the at least one firmware algorithm; and

the at least one PCM data stream is transmitted over a PSTN.

44. The system of claim 41, wherein the at least one data line comprises at least one bidirectional PCM data stream.

45. The system of claim 41, wherein the at least one data line comprises at least one bidirectional host bus.

46. The system of claim 41, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

determining a data type of the data received into at least one of the plurality of service DSP engines and determining at least one firmware algorithm required to process the data type;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available; and

unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

47. The system of claim 46, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

48. The system of claim 46, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is downloaded to each service DSP engine from the processor.

49. The system of claim 41, wherein the data received by the at least one of the plurality of DSP engines comprises at least one channel of multiplexed data received over a public switched telephone network, the data having at

least one of the plurality of data types comprising modem data, voice data, audio data, and facsimile data.

50. The system of claim 41, wherein each service DSP engine comprises at least one channel.

51. The system of claim 41, wherein at least one algorithm is transmitted on a channel of the serial bus.

52. The system of claim 41, wherein an algorithm is transmitted using at least one channel of the serial bus.

53. The system of claim 41, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms.

Sub A2

54. A computer readable medium containing executable instructions which, when executed in a processing system, causes the system to perform the steps for digital signal processing (DSP) of a plurality of data types comprising:

continuously broadcasting a plurality of firmware algorithms to a plurality of DSP engines over a channelized serial bus; and

selectively monitoring for and receiving at least one firmware algorithm of the plurality of firmware algorithms by at least one of the plurality of DSP engines, wherein the at least one firmware algorithm is used

to process data of at least one corresponding data type received by the at least one of the plurality of DSP engines over at least one data line.

55. The computer readable medium of claim 54, further causing the system to perform the steps of:

receiving at least one pulse coded modulation (PCM) data stream from a public switched telephone network (PSTN);

generating at least one packet of data from the PCM data stream using the received at least one firmware algorithm; and

transmitting the at least one packet of data over an Internet Protocol (IP) network.

56. The computer readable medium of claim 54, further comprising the steps of:

receiving at least one packet of data from an IP network;

generating at least one PCM data stream from the at least one packet of data using the at least one firmware algorithm; and

transmitting the at least one PCM data stream over a PSTN.

57. The computer readable medium of claim 54, wherein the system is caused to continuously broadcast the plurality of firmware algorithms to a plurality of service DSP engines by a master DSP engine resident in a processor.

58. The computer readable medium of claim 57, wherein the step of selectively monitoring for and receiving at least one firmware algorithm comprises the steps of:

determining a data type of the data received into at least one of the plurality of service DSP engines;

determining at least one firmware algorithm required to process the received data;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available.

59. The computer readable medium of claim 58, wherein the step of selectively monitoring for and receiving at least one firmware algorithm further comprises the step of unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

60. The computer readable medium of claim 59, wherein the step of selectively monitoring for and receiving at least one firmware algorithm further comprises the steps of:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

61. The computer readable medium of claim 54, wherein the processor is further configured so that data received by the at least one of the plurality of DSP engines comprises at least one channel of multiplexed data received over

a public switched telephone network, the data comprising modem data, voice data, audio data, and facsimile data.

62. The computer readable medium of claim 54, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms, wherein the broadcast of each of the at least one serial blocks is preceded by a broadcast of an address signal identifying the firmware algorithm of the broadcasted at least one serial block.

add C17 add D17